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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/767,065	01/29/2004	Toshiharu Furukawa	ROC920030268US1	5663

30206 7590 06/26/2009

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EXAMINER	
NADAV, ORI	

ART UNIT	PAPER NUMBER
2811	

MAIL DATE	DELIVERY MODE
06/26/2009	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/767,065	FURUKAWA ET AL.	
	Examiner	Art Unit	
	Ori Nadav	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 March 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6,8,25-28 and 34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6,8,25-28 and 34* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-6, 8 and 34 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The claimed limitation of a semiconductor device structure formed on a substrate defining a substantially horizontal plane, as recited in claim 1, is unclear as to which element defining a substantially horizontal plane.

The claimed limitation of a channel region being electrically insulated from said gate electrode, as recited in claim 1, is unclear as to how the gate electrode is electrically insulated from the substrate (the channel region), since all the elements in one semiconductor device are electrically connected to each other.

The claimed limitations of "said channel region" and "said gate electrode", as recited in claim 34, are unclear as to the structural relationship between the gate electrode and the semiconductor device.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-6, 8, 25-28 and 34, as best understood, are rejected under 35 U.S.C. 103(a) as being unpatentable over Choi et al. (6,566,704).

Regarding claims 25-28, Choi et al. teach in figure 3F and related text a semiconductor device structure formed on a substrate 200, the semiconductor device structure comprising:

an electrically conductive first plate 40 disposed on the substrate,

an electrically conductive second plate 50 disposed vertically above said first plate;

an electrically conductive layer 20 disposed between said first and second plates; at least one nanotube 100 having a first end electrically coupled with said first plate for increasing an effective area of said first plate and a second end, said at least one nanotube extending vertically through said electrically conductive layer from said first plate toward said second plate; and

a dielectric layer 30

wherein said dielectric layer having a first portion disposed between said one nanotube and said electrically conductive layer, and a second portion disposed between said one nanotube of said second plate,

wherein said at least one nanotube has a conducting molecular structure,

wherein said at least one nanotube has a semiconducting molecular structure, and

wherein said dielectric layer comprises a shell that encases said at least one nanotube, and

a gate dielectric layer 30, a respective one of said gate dielectric layer disposed between said channel region of said semiconducting nanotube and said gate electrode.

Choi et al. do not explicitly state in the embodiment of figure 3F a plurality of semiconducting nanotubes and plurality of dielectric layers.

Choi et al. teach using a plurality of semiconducting nanotubes in the disclosed invention of nano sized transistor (see, for example, column 3, lines 39-43), wherein figures 1-3 depict only a unit cell of the transistor (column 3, lines 41-43).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use a plurality of semiconducting nanotubes having a plurality of dielectric layers in Choi et al.'s device in order to use the device in a practical application which requires a plurality of semiconducting nanotubes having a plurality of dielectric layers, such as a nano sized transistor.

Regarding claim 1, Choi et al. teach in figure 3F and related text a vertical semiconductor device structure formed on a substrate 200 defining a substantially horizontal plane, the semiconductor device structure comprising:

a source region 40;

a drain region 50;

a gate electrode 20 disposed on the substrate, said gate electrode positioned vertically between said source region and drain region; and

a nanotube 100 including a first end physically and electrically coupled with said source region, a second end electrically coupled with said drain region, and a channel region extending vertically through said gate electrode between said source and drain regions, said channel region being electrically insulated from said gate electrode, and said gate electrode configured to receive a control voltage effective to regulate current flow through said channel region between said source region and said drain region.

Choi et al. do not explicitly state in the embodiment of figure 3F a plurality of semiconducting nanotubes.
Choi et al. teach using a plurality of semiconducting nanotubes in the disclosed invention of nano sized transistor (see, for example, column 3, lines 39-43), wherein figures 1-3 depict only a unit cell of the transistor (column 3, lines 41-43).
It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use a plurality of semiconducting nanotubes in Choi et al.'s device in order to use the device in a practical application which requires a plurality of semiconducting nanotubes, such as a nano sized transistor.

Regarding claims 4-6 and 8, Choi et al. teach in figure 1 and related text an insulating layer 30 disposed between said drain and said gate electrode for electrically isolating

said drain from said gate electrode, an insulating layer 10 disposed between said source and said gate electrode for electrically isolating said source from said gate electrode, wherein said at least one semiconducting nanotube is composed of arranged carbon atoms, wherein said at least one semiconducting nanotube is oriented substantially perpendicular to said horizontal plane.

Regarding claims 2-3, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to form the source and drain of a catalyst material effective for growing said at least one semiconducting nanotube in Choi et al.'s device in order to simplify the processing steps of making the device.

Note that the process limitations of forming the source and drain of a catalyst material effective for growing said at least one semiconducting nanotube, would not carry patentable weight in this claim drawn to a structure, because distinct structure is not necessarily produced. A "product by process" claim is directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17 (footnote 3). See also In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Fessmann, 180 USPQ 324; In re Avery, 186 USPQ 161; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); and In re Marosi et al., 218 USPQ 289, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in

"product by process" claims or not. Note that the applicant has the burden of proof in such cases, as the above case law makes clear.

Regarding claim 34, the combined device comprises a plurality of gate dielectric layers, wherein a respective one of said gate dielectric layers disposed between said channel region of one of said semiconducting nanotubes and said gate electrode.

Response to Arguments

Applicant argues that there is no motivation to form plurality of nanotubes in Choi's device, because "Choi fails to explicitly disclose or suggest that the dimensions of the hole (10') can be increased to accommodate multiple semiconducting nanotubes (100), much less that the hole (10') can accommodate more than one nanotube (100) without any modification in the dimensions". Applicant further argues that "the Examiner's conclusion that each unit cell shown in Figures 1-3 of Choi can include multiple semiconducting nanotubes is based solely upon the hindsight provided by Applicants' own specification". Applicant continues that "Even if a person having ordinary skill in the art were to replicate the single nanotube unit cell shown in Figures 1-3 of Choi to make multiple unit cells, each of the individual unit cells would still only include a single semiconducting nanotube (100) with a channel current flow regulated by a control voltage from a gate electrode (20)".

The combination is not based upon the hindsight, because Choi et al. teach a transistor using carbon nanotubes. Furthermore, the examiner does not suggest increasing the dimensions of the hole (10') to accommodate multiple semiconducting nanotubes (100). Since Choi et al. teach a transistor using carbon nanotubes, it is understood that Choi et al. teach plurality of unit cells. Although each of the individual unit cells would still include only a single semiconducting nanotube, the claimed limitation of "a channel region extending vertically through said gate electrode between said source and drain regions" means that only one channel region is located in the device and "said channel region" in the passage "gate electrode configured to receive a control voltage effective to regulate current flow through said channel region of each of said semiconducting nanotube between said source region and said drain region" refers back to the single channel region recited previously in the claim.

Applicant argues that "The intrinsic evidence in Choi fails to teach a person having ordinary skill in the art how to modify the device shown in Figures 1-3 to include a plurality of nanotubes. This is not an obvious modification that a person having ordinary skill in the art would have made to the device structure of Figure 3F based upon the Examiner's allegedly objective reasoning and with a reasonable expectation of success".

As explained above, the examiner does not suggest to modify the device structure of Figure 3F. The examiner suggests that plurality of unit cells are present in

the transistor of Choi et al., and it would be obvious for an artisan to form a transistor comprising plurality of carbon nanotubes, as is taught Choi et al.

Applicant argues on page 5 that "the Examiner apparently recognizes that each transistor in Choi includes a single nanotube". Since "Claim 1 recites that "each of said semiconducting nanotubes" includes "a channel region extending vertically through said gate electrode between said source region and said drain region" and the gate electrode regulates "current flow through said channel region between said source region and said drain region".", then "the semiconductor device structure in claim 1 has multiple channel regions", whereas "each semiconductor device structure in Choi includes one nanotube and one channel region".

The Examiner agrees that "each semiconductor device structure in Choi includes one nanotube and one channel region". However, said "each semiconductor device structure" in Choi is only one unit cell, and the final device structure comprises plurality of unit cells. Therefore, the final device structure of Choi multiple channel regions, as claimed.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP

§ 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ori Nadav whose telephone number is 571-272-1660. The examiner can normally be reached between the hours of 7 AM to 4 PM (Eastern Standard Time) Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Gurley can be reached on 571-272-4670. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published

applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

O.N.
6/26/2009

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